# Refine Search

Your wildcard search against 10000 terms has yielded the results below.
***Your result set for the last L# is incomplete.***
The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

**Search Results -**

| Terms | Documents |
|---|---|
| L13 same us$ | 35 |

**Database:**
US Pre-Grant Publication Full-Text Database
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Derwent World Patents Index
IBM Technical Disclosure Bulletins

**Search:** L14

Refine Search | Recall Text | Clear | Interrupt

## Search History

**DATE: Monday, June 07, 2004** Printable Copy Create Case

| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=USPT; PLUR=YES; OP=OR* | | | |
| L14 | L13 same us$ | 35 | L14 |
| L13 | mark$ same l7 | 97 | L13 |
| L12 | L10 and l4 | 0 | L12 |
| L11 | L10 same l4 | 0 | L11 |
| L10 | fuse adj1 map | 42 | L10 |
| L9 | L2 same l4 | 10 | L9 |
| L8 | L7 same l1 | 2 | L8 |
| L7 | redundant same (row or column) | 3867 | L7 |
| L6 | L4 and l1 | 6 | L6 |
| L5 | L4 same l1 | 0 | L5 |
| L4 | retest$ | 5070 | L4 |
| L3 | L2 and l1 | 13 | L3 |

| | | | |
|---|---|---|---|
| L2 | bisr or bist | 1400 | L2 |
| L1 | field adj1 repair$ | 1144 | L1 |

END OF SEARCH HISTORY

# Refine Search

**Search Results -**

| Terms | Documents |
|---|---|
| L1[ti,clm] | 17 |

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**Search:** L4

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## Search History

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| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=USPT; PLUR=YES; OP=OR* | | | |
| L4 | L1 [ti,clm] | 17 | L4 |
| L3 | L1 same memory | 1 | L3 |
| L2 | L1 same redundant | 0 | L2 |
| L1 | field adj1 repairable | 113 | L1 |

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# Refine Search

**Search Results -**

| Terms | Documents |
|---|---|
| L1 same redundant | 9 |

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**Search:** L4

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## Search History

**DATE: Monday, June 07, 2004** Printable Copy Create Case

| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=USPT; PLUR=YES; OP=OR* | | | |
| L4 | L1 same redundant | 9 | L4 |
| L3 | L1 same soc | 0 | L3 |
| L2 | L1 same memory | 28 | L2 |
| L1 | retest$ same packag$ | 146 | L1 |

END OF SEARCH HISTORY

L4: Entry 4 of 9 File: USPT May 16, 2000

DOCUMENT-IDENTIFIER: US 6065134 A
TITLE: Method for repairing an ASIC memory with redundancy row and input/output lines

Brief Summary Text (10):
A conventional solution provides repairing schemes that encompass a number of separately performed processes, each of which requires equipment that is external to the ASIC memory chip. The first of these processes is testing. Automatic Test Equipment (ATE) is used to test at least one memory array on an ASIC chip. A series of test signal patterns is applied through the ATE to detect the locations of memory failures based upon responsive outputs which are then recorded in the ATE. The next process is one of analysis. External software is used to determine optimal utilization of the redundant memory lines to repair the defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip for selective removal through conventional laser beam techniques to repair a defective memory cell. The final process involves retesting the chip using the ATE to ensure that the chip functions properly after being repaired. The repaired chip is then packaged and sent to the customer.

L4: Entry 5 of 9 File: USPT Jun 9, 1998

DOCUMENT-IDENTIFIER: US 5764878 A
TITLE: Built-in self repair system for embedded memories

Brief Summary Text (10):
A conventional solution provides repairing schemes that encompass a number of separately performed processes, each of which requires specific equipment that is external to the ASIC memory chip. The first of these processes is testing. Automatic Test Equipment (ATE) is used to test at least one memory array on an ASIC chip. A series of test signal patterns is applied through the ATE to detect the locations of memory failures based upon responsive outputs which are then recorded in the ATE. The next process is one of analysis. External software is used to determine optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip for selective removal through convention laser beam techniques to repair a defective memory cell. The final process involves retesting the chip using the ATE to ensure that the chip functions properly after being repaired. The repaired chip is then packaged and sent to the customer.

First Hit Fwd Refs

**End of Result Set**

Generate Collection Print

L3: Entry 1 of 1 File: USPT Mar 18, 1975

DOCUMENT-IDENTIFIER: US 3872291 A
TITLE: Field repairable memory subsystem

Brief Summary Text (4):
The invention relates generally to a memory subsystem for a data processing system, and more particularly, to a field-repairable store, in which basic units or arrays of store which are determined to be defective may be selectively disconnected from the store. A method of repairing a memory subsystem connected to a data processing system is also disclosed.

Detailed Description Text (20):
It will be apparent to those skilled in the art that the disclosed Field Repairable Memory Subsystem may be modified in numerous ways and may assume many embodiments other than the preferred form specifically set out and described above. For example, the initial testing of arrays after fabrication may be dispensed with, and all arrays may be initially activated (i.e., F5 turned on; or alternatively F5, Q10, Q12, and pad P1 removed from the Disconnect Control Circuit 120 entirely), and the memory subsystem may be tested solely in conjunction with the operating data processing system. According to this manner of array testing, the data processing system is programmed to sequentially address arrays within the memory subsystem, write data into the arrays, and read out such data to determine which arrays are defective. A listing of defective arrays can be generated, from which such arrays may be eliminated from the memory subsystem either manually or automatically by the data processing system. In this manner, a large portion of the costs associated with array testing can be eliminated, thus significantly reducing the per-bit cost of the memory subsystem.

L6: Entry 2 of 6 File: USPT Jan 7, 2003

DOCUMENT-IDENTIFIER: US 6505313 B1
TITLE: Multi-condition BISR test mode for memories with redundancy

Brief Summary Text (8):
To reduce repair costs and allow field repairs, some memory chips have been equipped with built-in self test (BIST) and built-in self repair (BISR) circuitry. The BIST circuit detects faults in the memory array and notifies the BISR circuit of the fault locations. The BISR circuitry generally reassigns the row or column containing the failing cell to a spare row or column in the memory array. BIST and BISR are typically performed each time power is applied to the system. This allows any latent failures that occur between subsequent system power-ups to be detected in the field.

CLAIMS:

1. A device which comprises: a reconfigurable component having redundant portions; a built-in self-test (BIST) unit coupled to the reconfigurable component and configured to test the reconfigurable component to identify faulty portions of the reconfigurable component; and a built-in self-repair (BISR) unit configured to store identifiers of the faulty portions and coupled to the reconfigurable component to configure the redundant portions to operate in lieu of the faulty portions, wherein the BIST unit is further configured to retest the reconfigurable component anew to identify faulty portions of the reconfigurable component at a subsequent time, wherein the BISR unit is further configured to receive subsequent identifiers of the faulty portions, and wherein the BISR unit is configured to compare the subsequent identifiers to the stored identifiers to identify any discrepancies; wherein said subsequent identifiers are stored by the BISR unit in a shift chain, and wherein the BISR unit is configurable to serially shift the contents of the shift chain to one or more external pins for off-chip examination; and wherein the stored identifiers are addresses stored in reserve latches, and wherein the subsequent identifiers are addresses stored in address latches, and the BISR unit includes logical XOR gates that perform bit-wise comparisons between the contents of the reserve and address latches to provide corresponding match signals to a detector that detects simultaneous assertion of all said match signals.

L9: Entry 1 of 10 File: USPT Apr 27, 2004

DOCUMENT-IDENTIFIER: US 6728910 B1
TITLE: Memory testing for built-in self-repair system

Abstract Text (1):
A method is presented for self-test and self-repair of a semiconductor memory device. A single built-in self-test (BIST) engine with an extended address range is used to test the entirety of memory (i.e., both redundant and accessible memory portions) as a single array, preferably using a checkerboard bit pattern. An embodiment of the method comprises two stages. In the first stage, faulty rows in each memory portion are identified and their addresses recorded. Known-bad rows in accessible memory are then replaced by known-good redundant rows, and the resulting repaired memory is retested in a second stage. During the second stage, repair of the accessible memory portion is verified, while defects among the redundant portion are ignored. Compared to existing methods, the new method is believed to simplify the interface between the BIST and the built-in self-repair (BISR) circuitry, reduce the overall size of test and repair circuitry, and provide improved test coverage.

Brief Summary Text (9):
A typical BIST/BISR method employs two BIST stages (also referred to herein as BIST "runs"). In the first stage, the accessible memory is tested row-by-row until a defect is encountered. The row containing the defect is then replaced by the first available redundant row and retested. This process continues until all of the accessible memory has been tested, or until there are no more redundant rows to use as replacements. In the first case, a second BIST run is performed, verifying all of the accessible memory. In the second case, the device is flagged as non-repairable. The two-stage method suffers from several drawbacks, among them the fact that it may overlook adjacent row interaction defects in the memory. Since the method tests accessible memory and redundant memory separately, it cannot detect interaction between adjacent accessible and redundant rows. A further disadvantage of the conventional two-stage method is that the total test time is not predictable. The duration of the test is dependent on the number of bad accessible memory rows, each of which has to be replaced and retested. Since there is no way to know the test time in advance, precise test scheduling during production is impossible.

Brief Summary Text (16):
The method disclosed herein may be used for self-test and self-repair of a memory comprising first and second arrays. According to this embodiment, the entirety of the memory is tested as a single addressable array, and rows in the first and second arrays that fail the test are detected. After the entire memory has been tested, failing rows from the first array are replaced with non-failing rows from the second array in a repair operation. The entirety of the memory is then retested as a single addressable array. During the retest, failing rows in the second array are ignored. If failing rows are detected in the repaired first array during the retest, a "fail" result is returned; otherwise, a "pass" result is returned. The first array represents the accessible portion of the memory and the second array the redundant portion. According to the method disclosed herein, testing of the memory is done during the first stage of a two-stage procedure, and retesting during the second stage. The repair operation consists of recording the addresses

of failing accessible rows in a repair table; associated with each of these addresses is the address of a non-failing redundant row. Using the repair table, the BISR dynamically substitutes a good redundant row for every failing accessible row.

Brief Summary Text (18):
In addition to the above-mentioned improved BIST/BISR method and computer-usable medium, a system for self-test and self-repair of a semiconductor memory is contemplated herein. In an embodiment, the system consists of a first m.times.n memory array, a second p.times.n memory array, a single built-in self-test (BIST) engine adapted to test the first and second arrays as a single joint array and detect rows failing the test, and built-in self-repair (BISR) circuitry that replaces failing rows in the first array with non-failing rows from the second array. The BIST is configured to generate row addresses that span the entire memory array (i.e., m+p rows). The BISR circuitry is capable of assigning addresses generated by the BIST that exceed the dimensions of the first array (i.e., >m) to rows in the second array. The BISR circuitry may also be capable of reassigning the addresses of failing rows in the first array to rows in the second array. The BIST may test the memory array in two test stages. In the first test stage, the addresses of rows that fail are recorded in a defect list. If there are enough non-failing rows in the second array at the end of the first test stage to replace all the failing rows from the first array, the memory is repaired and retested in a second stage. During the second stage, defects in the first array result in a "fail" test result, while defects in the second array are ignored. If there are no defects in the first array, a "pass" result is returned. Memory tests performed by the BIST may consist of writing a bit pattern to a portion of the memory, then reading back the contents and comparing them to the original bit pattern. A commonly used bit pattern, called a checkerboard, consists of alternating 1's and 0's.

Detailed Description Text (17):
In a second stage, the BIST may retest the memory, again generating row addresses from 0 to m+p-1. As it does so, the BISR monitors the addresses on mem_address bus 76. If an address is within the accessible memory (i.e., <m), the BISR compares it to the defective row addresses in its repair table. For each defective accessible row, the BISR substitutes the associated good redundant row. Thus, when the BIST retests the first m rows of the memory, it is actually testing a combination of accessible and redundant rows that tested good in the first stage. If an error occurs in the first m rows during the second stage, the memory is considered non-repairable, and the BISR toggles the externally-accessible FAIL flag 84. Addresses beyond the accessible memory (i.e., =m-1) are effectively omitted from testing. During the second stage, when the BISR detects an out-of-range address on mem_address bus 76, it suppresses the error flags ERRN 78 and FAIL 84. This is justifiable, since these addresses are not within the nominal address range of the memory device.

CLAIMS:

1. A system for self-test and self-repair of a semiconductor memory, said system comprising: a first portion of the memory, comprising an array of m rows and n columns; a second portion of the memory, comprising a array of p rows and n columns; test circuitry adapted to access the first and second portions as a single joint array comprising m+p rows and n columns, test the entirety of the joint array and detect rows failing the test, wherein the test circuitry comprises a single built-in self-test (BIST) engine having a fixed array size; repair circuitry adapted to replace failed rows in the first portion with non-failing rows from the second portion; and wherein the test circuitry is further adapted to retest the first and second portions of memory, while ignoring failing rows in the second portion.

L14: Entry 21 of 35 File: USPT Nov 3, 1992

DOCUMENT-IDENTIFIER: US 5161157 A
** See image for Certificate of Correction **
TITLE: Field-programmable redundancy apparatus for memory arrays

Detailed Description Text (26):
To mark a redundant row as being in non-functional or bad condition, the Mark Bad Redundant Row operation 308 shown in FIG. 5B is used. In this operation, the row number of the redundant row to be marked is supplied in encoded form on address lines A[6:4] along with a logic high on address line A[3] and a logic low value on address line A[0]. The remaining address lines and the data I/O lines are not used in this operation. The user must determine whether a redundant row is in functioning condition by first mapping it into a primary row address while in redundancy mode and then performing standard read/write test operations to the redundant row during normal mode.

Detailed Description Text (42):
Specifically, NOVRAM Bit Cell 520 provides a complementary "used" signal at port 532 which is fed into the tenth input of NOR gate 560. The "used" signal from port 532 functions in the same manner as any one of the bit match signals and will prevent a match signal at port 170 if Redundant Row Decoder 120 has not yet been programmed as a replacement for a bad primary row, or if it has been programmed into a disabled state by the Reset Redundant Row Address operation 307, shown in FIG. 5, described above. NOVRAM bit Cell 500 provides a disable signal at port 512 which is fed into the eleventh input of NOR gate 560. The disable signal is programmed to a logic high in Mark Bad Redundant Row Operation 308 if the correspond redundant row of Redundant Row Decoder 120 has been found to be non-functional. The disable signal from port 512 functions in the same manner as any one of the bit match signals and will prevent a match signal at port 170 if Redundant Row Decoder 120 has been marked as a bad redundant row.

Detailed Description Text (46):
During programming operations in the redundancy mode, for example operations 306-308 shown in FIG. 5B, NOVRAM Compare Cells 400-408 and NOVRAM Bit Cells 500 and 520 are programmed simultaneously. During the Program Redundant Row Address Operation 306 shown in FIG. 5B, the primary row address to be replaced by the redundant row corresponding to Redundant Row Decoder 120 is programmed into NOVRAM Compare Cells 400-408. In this operation, a low state is programmed into NOVRAM Bit Cell 500 to indicate that the row is in good condition, and a high state is programmed into NOVRAM Bit Cell 520 to indicate that the redundant row is now being used. During the Reset Redundant Row Address operation 307 shown in FIG. 5B, no information is programmed into NOVRAM cells 400-408, a low state is programmed into NOVRAM Bit Cell 500 to indicate that the redundant row is still functional, and a low state is programmed into NOVRAM Bit Cell 520 to indicate that the redundant row corresponding to Redundant Row Decoder 120 is not being used. For the Mark Bad Redundant Row operation 308 shown in FIG. 5B, no information is programmed into NOVRAM Compare Cells 400- 408, a high state is programmed into NOVRAM Bit Cell 500 to indicate the row is non-functional (bad), and no information is programmed into NOVRAM Bit Cell 520. This status information is later read out with the redundancy read Operations 304 and 305 so that the user can determine the mapping of redundant row to primary rows, the used redundant rows, and the bad redundant rows.

Detailed Description Text (83):
If, however, the given primary row to be replaced is currently replaced by a redundant row, the user must first nullify, or undo, the previous replacement before making the new replacement. The undoing of the previous replacement is shown at a block 1012 of FIG. 14 and is done with Reset Redundant Row Address operation 307 shown in FIG. 5B. In this operation, the address of the redundant row to be reset is given on address lines A[6:4] and address lines A[3:0] are set to their appropriate logic values. The row is then marked as a failed redundant row, as shown by a block 1014, with the Mark Bad Redundant Row operation 308 shown in FIG. 5B. In this operation, the address of the redundant row to be marked is given on address lines A[6:4] and address lines A[3:0] are set to their appropriate logic values. Once the bad redundant row has been marked, the user proceeds to block 1016 where the replacement of the failed row with a functional and available redundant row can be made. Once the replacement is made, the user may exit the redundancy mode as shown by a block 1018, with Exit Redundancy Mode operation 309 shown in FIG. 5B. In this operation, all address lines A[15:0] are set to a high value.